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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

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☐ Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (280 characters max)

SEAMLESS INTEGRATED OPTICAL WAVE GUIDE FOR LIGHT GENERATED BY A SEMICONDUCTOR LIGHT SOURCE

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(914) 333-9615

ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification Number of Pages

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4

☐ Other (specify)

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

☐ Applicant claims small entity status. See 37 CFR 1.27.

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The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE

Date

23 January 2004

REGISTRATION NO.: 48,027

(if appropriate)

TYPED or PRINTED NAME

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USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450

SEAMLESSLY INTEGRATED OPTICAL WAVE GUIDE FOR LIGHT GENERATED BY A SEMICONDUCTOR LIGHT SOURCE

BACKGROUND OF THE INVENTION

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1. Technical Field

The present invention relates generally to the transmission of data at the silicon level, and relates more specifically to a wave guide seamlessly integrated with a semiconductor light source of a different technology for conducting light generated
10 by the semiconductor light source.

2. Related Art

As computer chip technology continues to evolve, the ability to further enhance the processing and transmission performance of data at the silicon level
15 remains an ongoing challenge. Traditionally, information is processed and transmitted electrically over small metallic wires that interconnect silicon-based devices, such as transistors and/or other electrical components. However, transmitting electricity over wires is subject to certain limitations, including limited
transmission speeds, electromagnetic interferences, etc.

20

One potential solution to overcome some of the limitations of electrical transmission is to utilize pulsed light to carry information over an optical network. However, in order to implement such an optical network, systems are required: (1) for generating light at the silicon level, and (2) for transmitting the light from one device to another.

In the art, it is known that when a bipolar transistor is biased into avalanche, light is generated in the reverse biased collector-base diode. The amount of light can be tuned by both the collector-base voltage as well as the current through the device (unlike an avalanche diode, which is commonly used). This enables light generation at very low current densities. The substrate current can be a measure for the amount of generated light. The typical wavelength of the generated light is $\lambda < 1 \mu\text{m}$ (i.e., near-infrared light for lightly-doped silicon). Figure 1 depicts an example of a model for generating light from a bipolar transistor, where E is the emitter, C is the collector, B is the base, and SUB is the measure of substrate current. Details of such an embodiment are described, for instance, in J.H. Klootwijk, J.W. Slotboom, M.S. Peter, *Photo Carrier Generation in Bipolar Transistors*, IEEE Trans. Electron Devices, Vol. 49 (No. 9), pp. 1628, 2002, September 2002, which is hereby incorporated by reference.

In addition, other semiconductor light sources are known. One such example includes a laser diode.

Unfortunately, no effective solution exists for conducting light from the semiconductor light source to other locations in silicon. Moreover, specific control over the wavelength of the emitted light is limited to the material used to form the semiconductor light source. Therefore, limitations exist with regard to the types of materials that can be used and wavelengths that can be generated. Accordingly, a need exists for a system and method for conducting light at selected wavelengths from a semiconductor light source to other devices in the silicon.

SUMMARY OF THE INVENTION

The present invention addresses the above-mentioned problems, as well as others by providing an integrated optical wave guide for conducting light generated by a semiconductor light source. In a first aspect, the invention provides a seamlessly integrated hybrid optical network device, comprising: a semiconductor light source mounted in a cavity in a silicon substrate, wherein the semiconductor light source can be biased into an avalanche condition to emit photons, and wherein the semiconductor light source is fabricated from a non-silicon material; and a photonic bandgap (PBG) structure seamlessly integrated with the semiconductor light source to act as an optical wave guide for the photons emitted by the semiconductor light source, wherein the PBG structure is etched directly in the silicon substrate.

In a second aspect, the invention provides a method of fabricating a seamlessly integrated hybrid optical network device, comprising: providing a silicon substrate; etching a cavity in the silicon substrate; etching a photonic bandgap (PBG) structure in the silicon substrate proximate the cavity; and placing a non-silicon semiconductor light source in the cavity, wherein the semiconductor light source can be biased into an avalanche condition to emit photons.

In a third aspect, the invention provides a seamlessly integrated optical network, comprising: a non-silicon semiconductor light source mounted in a silicon substrate that can be biased into an avalanche condition to emit photon pulses; a photonic bandgap (PBG) structure fabricated in the silicon substrate and seamlessly integrated with the semiconductor light source in the silicon substrate that acts as an optical wave guide for the photon pulses generated by the semiconductor light source; and a receiving device realized proximate a distal end of the optical wave guide for receiving the photon pulses generated by the semiconductor light source.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

Figure 1 depicts a bipolar transistor reverse biased into an avalanche condition to emit photons in accordance with the present invention.

Figure 2 depicts a first step for forming an optical network device in accordance with the present invention.

Figure 3 depicts a side view of an optical network device in accordance with the present invention.

Figure 4 depicts a silicon based optical network in accordance with the present invention.

Figure 5 depicts four cross-sectional micrographs of exemplary photonic band gap (PBG) structures in a silicon wafer after dry etching with a mask.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a seamlessly integrated optical network comprising an optical wave guide structure that is combined with a semiconductor light source, resulting in a low-current density light source with a seamlessly integrated optical wave guide. In particular, the optical network comprises an optical wave guide structure etched into a silicon substrate and a light emitting device formed from a semiconductor material that resides in a cavity etched proximate the optical wave guide structure. Thus, light generated in the semiconductor light source can be

transported through a silicon wafer, and serve as a basic element/structure in an optical network.

The present invention utilizes "photonic bandgap" (PBG) structures to act as optical wave guides for light generated by the semiconductor light source. The PBG structures comprise corrugated channel-cage structures, which may for example be dry-etched in a silicon substrate. In an exemplary embodiment, PBG structures are implemented as two-dimensional (2D) crystals consisting of parallel cylinders (or elements) that can be readily realized at submicron lengths. Alternatively, as technology advances, photonic crystals with three-dimensional (3D) periodicity could likewise be utilized. A more complete discussion of PBG structures can be found, e.g., in U.S. Patent 5,987,208, "Optical Structure and Method for its Production," issued to Gruning et al., on Nov. 16, 1999, which is hereby incorporated by reference.

Figures 2 and 3 depict an exemplary method for implementing an optical network device 20. In the first step shown in Figure 2, a combined etching is performed to form both a cavity 41 and a PBG structure 22 in a silicon (e.g., BICMOS or CMOS) substrate 11. Using known techniques, corrugated channel-cage elements, i.e., the photonic bandgap (PBG) structures, can be readily etched in, for instance, a high-ohmic silicon wafer.

In the second step shown in Figure 3, a semiconductor light source 10 - in this case a bipolar device - formed from a different (e.g., non-silicon based) technology is placed into the cavity 41. It is understood that any type of semiconductor light source, e.g., transistors, laser diodes, etc., could be utilized as a light source and be placed into the cavity 41. Preferably, the semiconductor light source is fabricated from a material that is not purely silicon (Si), but is instead fabricated from a "non-silicon" material. Exemplary materials for the "non-silicon" semiconductor light

sources include, e.g., SiGe, SiGeC, InP, GaAs, etc. (Accordingly, the term "non-silicon" as used herein should be interpreted to include silicon compounds.)

The result is a hybrid optical network device 20 in which compound materials forming a semiconductor light source 10 are seamlessly integrated with a silicon-based optical waveguide 22. Depending on the material selected for the bipolar semiconductor light source 10, a specific wavelength (or different wavelengths) can be achieved that will be conducted by the PBG structure 22. Thus, the designer can select a desired light wavelength by using a material having properties to achieve the desired light wavelength. After adding the semiconductor light source 10 into the cavity 41 within silicon substrate 11, an interconnect layer 46 can be added.

Thus, a light source, e.g., of infrared light having a wavelength $\lambda < 1 \mu\text{m}$, is provided using a hybrid combination of semiconductor light sources and PBG structures, which are seamlessly integrated to form an optical network device 20 in, e.g., lightly doped silicon.

Referring to Figure 4, a top view of an optical network 13 is shown that includes a plurality of devices 10, 27a-d that communicate optically within a silicon substrate 11. Optical communication is achieved with the optical network device 20 described above in Figure 3 formed into silicon substrate 11. Device 20 includes: (1) a non-silicon semiconductor light source 10, in this case a bipolar transistor, capable of emitting a light beam 12, i.e., photon beam, from a base-collector junction, and (2) a PBG structure 22 having a plurality of PBG elements 14 that defines a wave guide channel 16. As can be seen, the light beam 12 can be "bent" and split through the wave guide channel 16, thereby allowing the light source to be directed to any point in the silicon substrate 11. PBG elements 14 can therefore be strategically located as needed throughout the silicon substrate 11 to create any desired wave guide

configuration. Possible configurations may include wave guides channels with beam splitters to achieve multiple branches, configurations for achieving polarization and/or filtering, channels that interconnect devices internally within the silicon substrate 11, channels that interconnect devices with external devices, etc.

- 5 In the exemplary embodiment shown in Figure 4, the wave guide is connected to a set of receiving devices 27a-d (e.g., photo-diodes) that receive pulsed light from the semiconductor light source 10. Control over the network 13 can be provided by control system 29, which may include, e.g., a microprocessor or other logic that dictates when light should be transmitted from the semiconductor light source.
- 10 Control system 29 may reside within the silicon substrate 11 and/or externally to the substrate.

- To increase the effectiveness of the emitted light, semiconductor light source 10 may be fabricated with a reflective material 25 (e.g., a $\frac{1}{2}$ λ -coating) on one or more surfaces to block photon emission and thereby cause the light beam 12 to be directed
- 15 out of only a single surface. Furthermore, the reflective material 25 could be selectively placed to define an optical window 24 through which the light source will be focused.

PBG Structure

- 20 Figure 5 depicts four cross-sectional micrographs of exemplary photonic band gap (PBG) structures in a silicon wafer after dry etching with a mask. Each cylinder element essentially comprises a "pore" through the silicon. In these four embodiments, the mask hole diameter and pitch are (a) 2 μm and, 10 μm , (b) 1.5 μm and 3.5 μm , (c) and (d) 3 μm and 5 μm . Obviously, the particular diameter and pitch
- 25 of the PBG structure 22 can vary according to the particular application. In addition,

it should be understood the PBG structure 22 could be fabricated with a wet chemical etch process.

Typically the pores in the PBG structure 22 have a round cross section and are arranged in a square or hexagonal array to make the structure suitable for guiding polarized light and non-polarized light, respectively. Exemplary pore diameters are of the order of $1\text{ }\mu\text{m}$, and the pitch a between the pores is only slightly larger. The wavelength λ can be tailored by setting the pitch a , the relationship being: $a/\lambda = 0.2$ to 0.5 . This implies that a complete wavelength range can be covered from the near to the far infrared, e.g., $0.8\text{ }\mu\text{m}$ (GaAs bandgap) and 1.1 (Si bandgap) to $\sim 100\text{ }\mu\text{m}$. Example: for $\lambda = 5\text{-}6\text{ }\mu\text{m}$, pitch $a = 1.5\text{-}2.5\text{ }\mu\text{m}$. Typical characteristic pore diameter and pitch values for a PBG structure can be, depending on the wavelength of the light to be guided, of the order of 300 nm (for visible light guiding) to a few μm (for infrared light guiding).

Any methodology may be employed to realize the PBG structure 22. One way of manufacturing the PBG structure is by electrochemical etching, e.g. photo-electrochemical etching of lightly n-doped silicon, with the silicon wafer connected as the anode. By varying the photo-irradiation intensity of the wafer backside, i.e., the current density, during the electrochemical etching the pore radius can be changed periodically.

The pore array that makes up the PBG structure 22 could also be realized by using dry etching, i.e., reactive ion etching (RIE). In addition, the PBG structure 22 could be realized with the corrugated pillars remaining, thus creating the inverse structure of an array of pillars instead of pores.

One dry-etching technique for making the necessary corrugated pore array structures involves the so-called "Bosch process." This process is a dry-etching

process enabling high aspect ratio trenches and pores. Etching is done in SF_6 chemistry whereas passivation is done in C_4F_8 chemistry. By changing the process parameters such that one alternatively enters and leaves the process window from anisotropic into isotropic etching, these corrugated structures can be made. The silicon etch process is based on plasma etching where rapidly switching of etching and passivation chemistry enables the formation pores, trenches, etc.

An exemplary process may use the following steps:

- (1) Etching and passivation as in the Bosch process, until the desired depth of the first corrugation.
- (2) Step 1 ends with an etch cycle. This is required since the passivation polymer on the bottom of the pore has to be removed in order to enable the next isotropic etching step.
- (3) Isotropic etching by using SF_6/O_2 chemistry. During the isotropic step the platen power (bias voltage on the chuck supporting the wafer) is switched off to reduce the ion-assisted etching and to maximize the chemically assisted etching by radicals and neutrals, and thus to improve isotropic etching of silicon.
- (4) After the isotropic etch step, the process switches to the next step, starting this time with a passivation cycle; this to cover and protect the complete structure etched thus far with a passivation layer. Next, the process resumes step 1 again and can be repeated several times.

Generally speaking, the optical wave guide may consist of a high refractive index core with a lower refractive index cladding. Typical combinations that can be use include: TiO_2 core and SiO_2 cladding; Si_3N_4 core and SiO_2 cladding; SiON core and SiO_2 cladding; PMMA core and Cr cladding; Poly Si core and SiO_2 cladding; and InGaAsP core and InP cladding.

Semiconductor light source

As noted, the semiconductor light source 10 can be fabricated from any non-silicon material suitable for providing the desired wavelength. Examples include

5 SiGe, SiGeC, InP, and GaAs.

It should be also noted that the non-silicon material could be mounted in any suitable type of silicon substrate, including an active substrate such as CMOS, high-speed SiGe, SiGeC, BiCMOS, etc. Any technique may be utilized to achieve this hybrid integration. One exemplary method starts with a high-resistivity wafer having

10 a thermal oxide layer e.g. 1 μm . A thick resist mask (e.g., 10 μm) is applied which defines "the cavity." After the oxide has been etched, the silicon is etched to the depth of the light-emitting device that will be placed in the cavity. Dry etching of cavities with nearly perfect sidewall slopes is possible using the BoschTM process in a commercially available etcher. The next step is the placement and the gluing of the

15 bipolar device in the cavity, using, e.g., an organic polymer glue, such as benzo cyclobutane (BCB). Next, a resist mask is applied and contacts are etched through the BCB layer to the bond pads of the recessed light-emitting device. A metal layer can then be deposited and structured to interconnect the light-emitting device with different IC devices.

20 The foregoing description of the preferred embodiments of the invention has been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teachings. Such modifications and variations that are apparent to a person skilled in the art are

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intended to be included within the scope of this invention as defined by the accompanying claims.

**SEAMLESS INTEGRATED OPTICAL WAVE GUIDE FOR LIGHT
GENERATED BY A BIPOLAR TRANSISTOR**

BACKGROUND OF THE INVENTION

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A seamlessly integrated hybrid optical network device. The device comprises:
a semiconductor light source (10) mounted in a cavity in a silicon substrate (11),
wherein the semiconductor light source (10) is fabricated from a non-silicon material;
and a photonic bandgap (PBG) structure (22) seamlessly integrated with the
10 semiconductor light source (10) to act as an optical wave guide for the photons
emitted by the semiconductor light source (10), wherein the PBG structure (22) is
etched directly in the silicon substrate.

CLAIMS

1. A seamlessly integrated hybrid optical network device (20), comprising:
a semiconductor light source (10) mounted in a cavity in a silicon substrate
5 (11), wherein the semiconductor light source (10) is fabricated from a non-silicon material; and
a photonic bandgap (PBG) structure (22) seamlessly integrated with the semiconductor light source (10) to act as an optical wave guide for the photons emitted by the semiconductor light source (10), wherein the PBG structure (22) is
10 etched directly in the silicon substrate (11).
2. The seamlessly integrated hybrid optical network device (20) of claim 1, wherein the semiconductor light source (10) includes a surface covered in a reflective material (25) that blocks emission of photons through the surface.
- 15 3. The seamlessly integrated hybrid optical network device (20) of claim 2, wherein the surface includes an optical window (24) that allows photons to pass from the semiconductor light source (10) to the surrounding silicon substrate.
- 20 4. The seamlessly integrated hybrid optical network device (20) of claim 3, wherein the PBG structure (22) includes a plurality of porous columns realized in the silicon substrate adjacent to the optical window defined on the surface of the semiconductor light source (10).

5. The seamlessly integrated hybrid optical network device (20) of claim 4, wherein the plurality of porous columns are arranged to define a channel that provides the wave guide for the photons emitted through the optical window.
- 5 6. The seamlessly integrated hybrid optical network device (20) of claim 1, wherein the emission of light from the semiconductor light source is regulated by a control system.
7. The seamlessly integrated hybrid optical network device (20) of claim 1, wherein
10 the semiconductor light source (10) is fabricated from a material selected from the group consisting of: SiGe, SiGeC, InP, and GaAs.
8. The seamlessly integrated hybrid optical network device (20) of claim 1, wherein the silicon substrate is fabricated from a material selected from the group consisting
15 of: CMOS, high-speed SiGe, SiGeC, and BiCMOS.
9. The seamlessly integrated hybrid optical network device (20) of claim 1, wherein the semiconductor light source (10) comprises a bipolar transistor that can be biased into an avalanche condition to emit photons.

10. A method of fabricating a seamlessly integrated hybrid optical network device (20), comprising:

- providing a silicon substrate (11);
- etching a cavity (41) in the silicon substrate;
- 5 etching a photonic bandgap (PBG) structure (22) in the silicon substrate (11) proximate the cavity (41); and
- placing a non-silicon semiconductor light source (10) in the cavity (41).

11. The method of claim 10, wherein the silicon substrate is fabricated from a material selected from the group consisting of: CMOS, high-speed SiGe, SiGeC, and BiCMOS.

12. The method of claim 10, wherein the semiconductor light source (10) is fabricated from a material selected from the group consisting of: SiGe, SiGeC, InP, and GaAs.

13. The method of claim 10, wherein the PBG structure (22) includes a plurality of porous columns arranged to define a channel that provides the wave guide for the photons emitted from the semiconductor light source.

14. The method of claim 10, wherein the semiconductor light source (10) comprises a bipolar transistor that can be biased into an avalanche condition to emit photons.

15. A seamlessly integrated optical network (13), comprising:

a non-silicon semiconductor light source (10) mounted in a silicon substrate

(11);

a photonic bandgap (PBG) structure (22) fabricated in the silicon substrate

5 (11) and seamlessly integrated with the semiconductor light source (10) in the silicon substrate (11) that acts as an optical wave guide for photon pulses generated by the semiconductor light source (10); and

a receiving device (27a-d) realized proximate a distal end of the optical wave guide for receiving the photon pulses generated by the semiconductor light source

10 (10).

16. The seamlessly integrated optical network of claim 15, further comprising a control system (29) for regulating the emission of photon pulses from the semiconductor light source (10).

15

17. The seamlessly integrated optical network of claim 15, wherein the receiving device comprises a photo diode.

18. The seamlessly integrated optical network of claim 15, wherein the semiconductor
20 light source (10) includes a surface covered in a reflective material (25) that blocks emission of photons pulses through the surface.

19. The seamlessly integrated optical network of claim 18, wherein the surface
includes an optical window (24) that allows photon pulses to pass from the
25 semiconductor light source (10) to the surrounding silicon substrate (11).

20. The seamlessly integrated optical network of claim 19, wherein the PBG structure (22) includes a plurality of porous columns realized in the silicon substrate adjacent to the optical window defined on the surface of the semiconductor light source (10).

5

21. The seamlessly integrated optical network of claim 15, wherein the semiconductor light source (10) is fabricated from a material selected from the group consisting of: SiGe, SiGeC, InP, and GaAs.

10 22. The seamlessly integrated optical network of claim 15, wherein the silicon substrate is fabricated from a material selected from the group consisting of: CMOS, high-speed SiGe, SiGeC, and BiCMOS.

23. The seamlessly integrated optical network of claim 15, wherein the semiconductor
15 light source (10) comprises a bipolar transistor that can be biased into an avalanche condition to emit photon pulses.

20

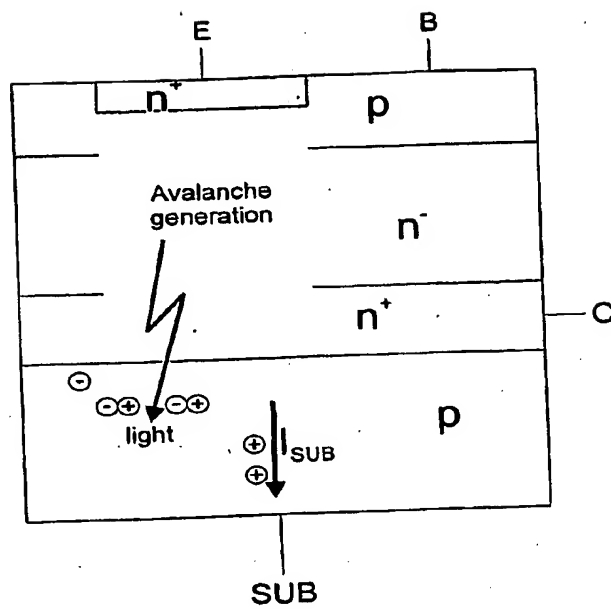


FIG. 1

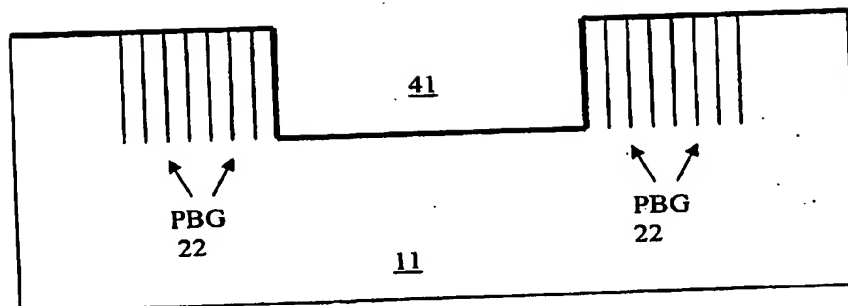


FIG. 2

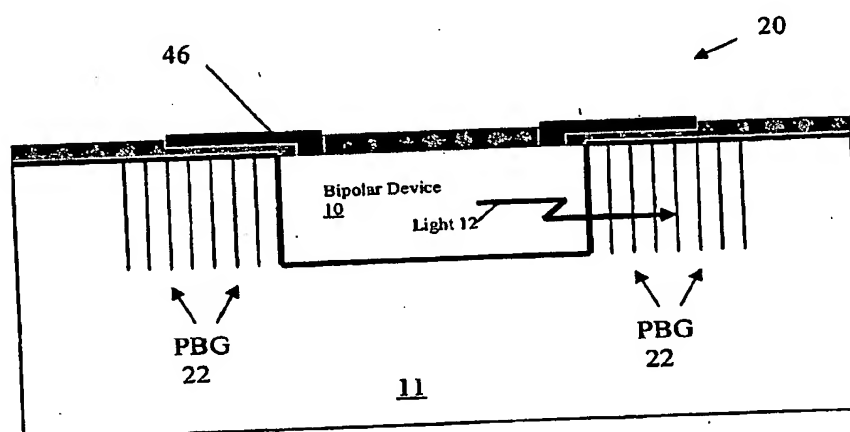


FIG. 3

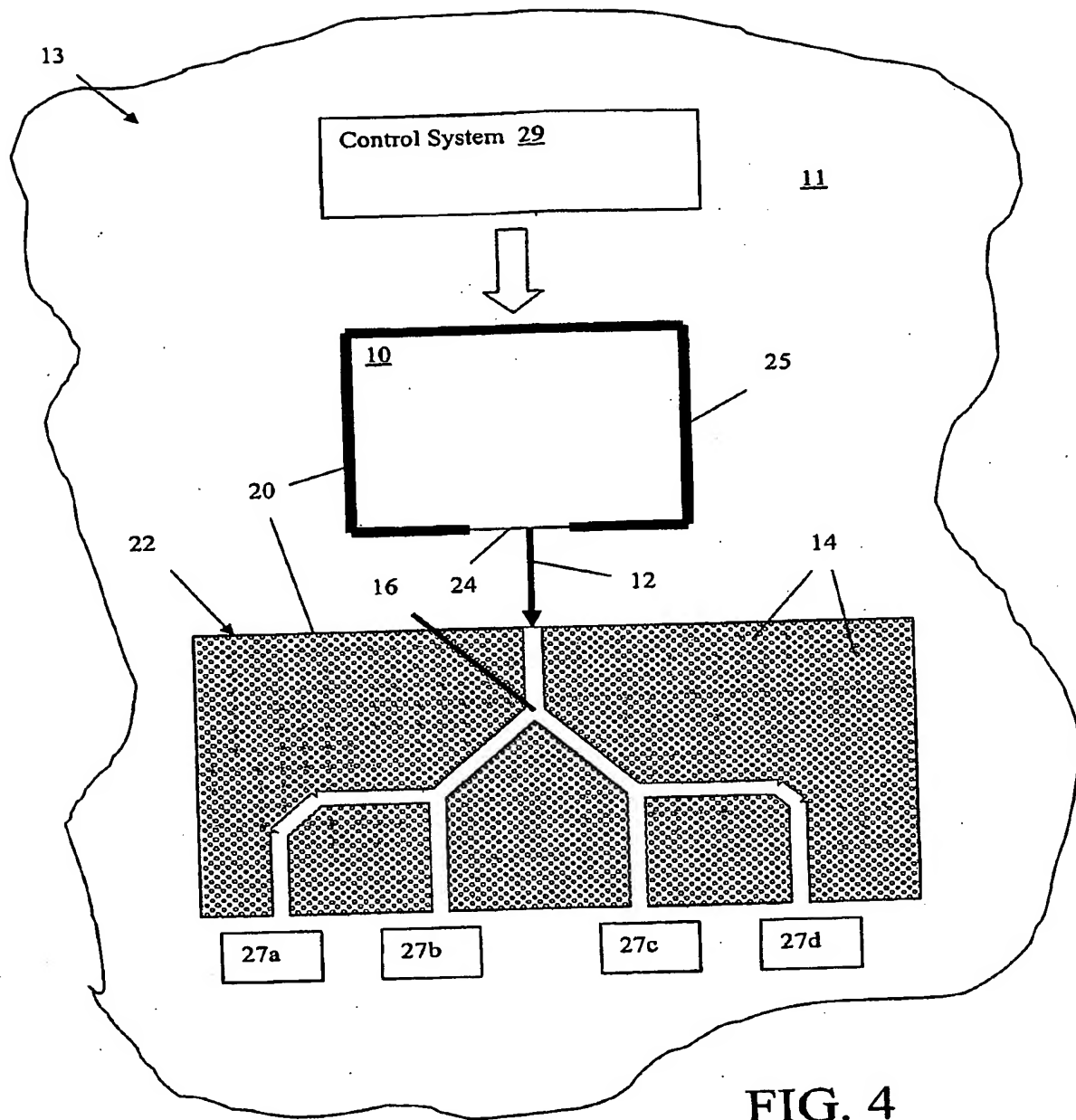


FIG. 4

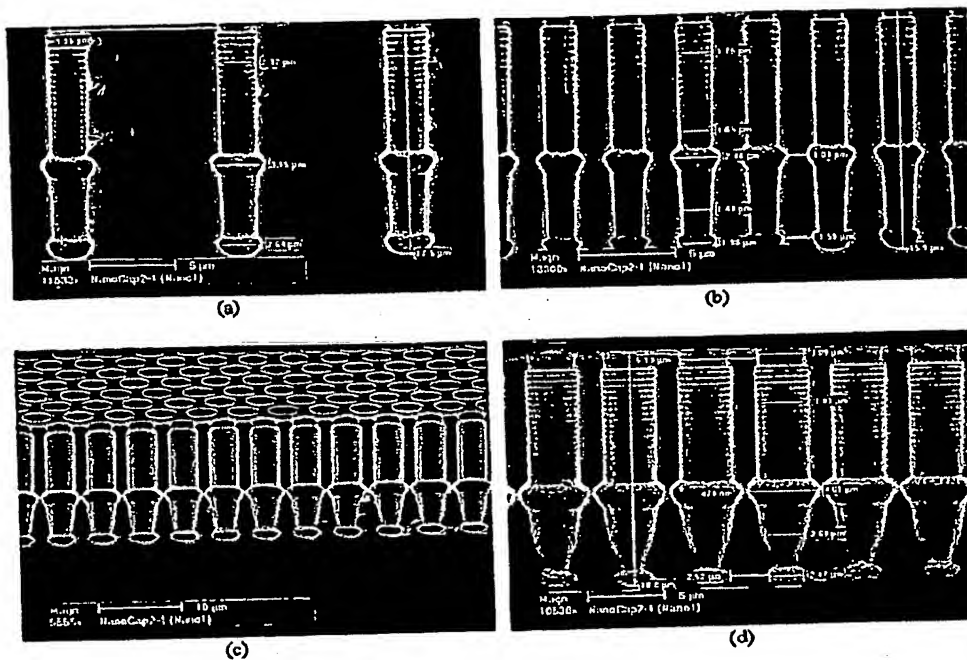


FIG. 5